Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims

1. (currently amended) A circuit for reducing adjacent pixel interdependence in a liquid crystal display, comprising:

a decomposer for dividing an input video signal into a plurality of signals having at least a high brightness signal and a low brightness signal;

a split low pass filter arrangement for independently low pass filtering rising transients and lengthening a fall time of falling transients in said low brightness signal to reduce adjacent pixel interdependence, wherein the split low pass filter arrangement comprises at least two low pass filters at least one of which is comprised of asymmetrically weighted taps thereby anticipating a bright-going signal and starting the bright-going signal going brighter earlier, at least one associated delay circuit, and a maximum selector circuit; and,

a delay matching circuit for the high brightness signal; and

means for combining the delayed high brightness signal with the filtered low brightness signal to provide an output with reduced sparkle artifacts.

2. (cancel)

3. (previously presented) The circuit of claim 1, wherein the at least two low pass filters and at least one associated delay circuit comprise a first low pass filter circuit, a second low pass filter circuit with an associated delay circuit, and a third low pass filter circuit with

another associated delay circuit, wherein the maximum selector circuit selects the maximum of the first, second, or third low pass filter circuits.

4. (original) The circuit of claim 3, wherein the second low pass filter circuit is symmetrical with a linear phase response.

5. (original) The circuit of claim 1, wherein the liquid crystal display is a liquid crystal on silicon (LCOS) display.

6. (original) The circuit of claim 3, wherein the third low pass filter circuit comprises an asymmetric 5-tap filter with coefficients 8/16, 4/16, 2/16, 1/16, and 1/16 preceded by a delay of 4 sample periods.

7. (original) The circuit of claim 3, wherein the first low pass filter comprises an asymmetric 5-tap filter with coefficients 1/16, 1/16, 2/16, 4/16, and 8/16.

8. (original) The circuit of claim 3, wherein the second low pass filter comprises a symmetric 3-tap filter with coefficients 3/16, 10/16, and 3/16, preceded by a delay of 3 sample periods.

9. (currently amended) A method for reducing adjacent pixel interdependence in a liquid crystal display, comprises the steps of:

dividing an input video signal into at least a high brightness signal and a low brightness signal;

low pass filtering said low brightness signal according to a first filtering rate to generate a first filtered value;

delay matching and low pass filtering said low brightness signal according to a second filtering rate to generate a second filtered value;

selecting as a filtered output for use in said combining step the maximum of said first and second filtered values;

independently low pass filtering rising transients and falling transients in said low brightness signal to reduce adjacent pixel interdependence said low-pass filtering comprising an asymmetrically weighted low-pass filter;

delay matching the high brightness signal with said filtered low brightness signal; and,

combining the delay matched high brightness signal and the filtered low brightness signal to provide an output signal with reduced sparkle artifacts.

10. (cancel)

11. (previously presented) The method of claim 9, wherein said low pass filtering step comprises the steps of

delay matching and low pass filtering said low brightness signal according to a third filtering rate to generate a third filtered value; and

selecting as a filtered output for use in said combining step the maximum of said first, second and third filtered values.

12. (original) The method of claim 9, wherein said low pass filtering step comprises the step of changing the shape of rising and falling pulses edges in said low brightness signal.

13. (currently amended) A circuit for reducing adjacent pixel interdependence in a liquid crystal display, comprising:

a decomposer comprising:

an input for receiving a video signal comprising respective samples of pixel brightness values;

at least a high brightness output providing consecutive high brightness value samples and a low brightness output providing consecutive low brightness value samples;

said consecutive low pixel brightness value samples defining pulses;

a filter coupled to said low brightness output, wherein the filter comprises at least two low pass filters at least one of which is comprised of asymmetrically weighted taps, at least one associated delay circuit, and a maximum selector circuit; and,

said filter adjusting transition times of said pulses so as to reduce adjacent pixel interdependence.

14. (previously presented) The circuit of claim 1 further comprising a combiner coupled to said filter and to said high brightness output for combining said high brightness samples with filtered low brightness samples to provide a filtered video signal having reduced adjacent pixel interdependence.

15. (currently amended) A method for reducing adjacent pixel interdependence in a liquid crystal display, comprises the steps of:

providing a video signal comprising respective samples of pixel brightness values;

decomposing said video signal to provide a first video signal portion comprising consecutive high brightness value samples and a second video signal portion comprising consecutive low brightness value samples;

said consecutive low pixel brightness value samples defining pulses; and

filtering said second video signal portion according to a first filtering rate to generate a first filtered value, and delay matching and filtering said second video signal portion according to a second filtering rate to generate a second filtered value, said second video signal portion being filtered by an asymmetrically weighted filter to adjust transition times of said pulses so as to reduce adjacent pixel interdependence.

16. (previously presented) The method of claim 15 further comprising steps of:

delaying said first video signal portion; and

combining said delayed first video signal portion with said filtered second video signal portion so as to provide a combined video signal having reduced adjacent pixel interdependence.